

0404

INFORMATION DISCLOSURE CITATION

| | | | |
|------------------|---------------------|-----------------|------------|
| Atty. Docket No. | 04329.3299 | Application No. | 10/829,182 |
| Applicants | Tsutomu SATO et al. | | A. WILSON |
| Filing Date | April 8, 2004 | Group: | 2819 |

U.S. PATENT DOCUMENTS

| Examiner Initial* | Document Number | Issue Date | Name | Class | Sub Class | Filing Date If Appropriate |
|-------------------|-----------------|----------------|----------------|-------|-----------|----------------------------|
| CU | 6,570,217 | May 27, 2003 | T. Sato et al. | — | — | — |
| CU | 6,100,132 | August 8, 2000 | T. Sato et al. | — | — | — |
| CU | 6,552,380 | April 22, 2003 | T. Sato et al. | — | — | — |
| | | | | | | |

FOREIGN PATENT DOCUMENTS

| | Document Number | Publication Date | Country | Class | Sub Class | Translation Yes or No |
|----|-----------------|--------------------|---------|-------|-----------|-----------------------|
| CU | 2000-58780 | February 25, 2000 | Japan | — | — | Abstract |
| | 10-256362 | September 25, 1998 | Japan | | | Abstract |
| | 2000-12858 | January 14, 2000 | Japan | | | Abstract |
| | 2001-257358 | September 21, 2001 | Japan | | | Abstract |
| | 2001-144276 | May 25, 2001 | Japan | | | Abstract |
| | 2002-324836 | November 8, 2002 | Japan | | | Abstract |
| | 2-280381 | November 16, 1990 | Japan | | | Abstract |
| | 60-150644 | August 8, 1985 | Japan | | | Abstract |
| CU | 63-278375 | November 16, 1988 | Japan | — | — | Abstract |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | |
|----|---|
| CU | T. Sato et al., "A New Substrate Engineering for the Formation of Empty Space in Silicon (ESS) induced by Silicon Surface Migration", IEDM Technical Digest, pp. 517-520, (1999) * |
| | T. Sato et al., "SON(Silicon on Nothing) MOSFET using ESS(Empty Space in Silicon) Technique for SoC Applications", IEDM Technical Digest, pp. 809-812, (2001) * |
| | T. Sato et al., "ESS(Empty Space in Silicon) SON(Silicon on Nothing). A New Substrate Engineering for the Formation of Empty Space in Silicon (ESS) induced by Silicon Surface Migration", Japan Society of Applied Physics, Silicon Technology, No. 14, pp. 61-65. (2000) JAN 2000 |
| | T. Sato et al., "Trench Transformation Technology using Hydrogen Annealing for Realizing Highly Reliable Device Structure with Thin Dielectric Films", 1998 Symposium on VLSI Technology, Digest of Technical Papers, pp. 206-207, (1988) * |
| CU | S. Matsuda et al., "Novel Corner Rounding Process for Shallow Trench Isolation utilizing MSTs (Micro-Structure Transformation of Silicon)", IEDM Technical Digest, pp. 137-140, (1998) * |

* No month cited in doc.

INFORMATION DISCLOSURE CITATION

| | |
|--------------------------------|----------------------------|
| Atty. Docket No. 04329.3299 | Application No. 10/820,182 |
| Applicants Tsutomu SATO et al. | |
| Filing Date April 8, 2004 | Group: 2819 |

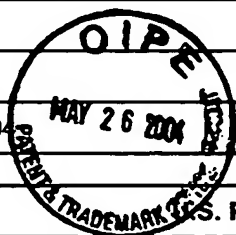
| OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) | |
|--|---|
| Q ne | T. Sato et al., "Discussion about dissolution of COP Defects by Direct Observation of Intentionally Grown Large Vacancy", Japan Society of Applied Physics, Extended Abstracts (The 60 th Autumn Meeting, 1999), 2p-S-17, p. 355, (1999) * |
| | T. Sato et al., "ESS(Empty Space in Silicon) SON(Silicon on Nothing). A New Substrate Engineering using Silicon Surface Migration(1) SON Structure realized by ESS", Japan Society of Applied Physics, Extended Abstracts (The 47 th Spring Meeting, 2000), 31a-YK-6, p. 888, (2000) * |
| | T. Sato et al., "ESS(Empty Space in Silicon). A New Substrate Engineering using Silicon Surface Migration(2) Design Guide for ESS Fabrication", Japan Society of Applied Physics, Extended Abstracts (The 47 th Spring Meeting, 2000), 31a-YK-7, p. 889, (2000) * |
| | T. Sato et al., "Theoretical Study on the Formation Process of Empty Space in Silicon", Japan Society of Applied Physics, Extended Abstracts (The 47 th Spring Meeting, 2000), 31a-YK-8, p. 889, (2000) * |
| | I. Mizushima et al., The Surface Science Society of Japan, 19 th , p. 14, (1999) * |
| | M. Kito et al., "Semiconductor Device and Manufacturing Method Thereof", U.S. appln. no. 09/549,513, filed April 14, 2000 |
| | T. Sato et al., "Semiconductor Substrate and its Fabrication Method", U.S. appln. no. 09/650,748, filed August 30, 2000 |
| | A. Yagishita, "Semiconductor Device and Manufacturing Method Thereof", U.S. appln. no. 10/436,181, filed May 13, 2003 |
| Q ne | K. Inoh, "Semiconductor Device with a Cavity therein and a Method of Manufacturing the same", U.S. appln. no. 10/665,614, filed September 19, 2003 |

| | |
|---|---|
| Examiner Q ne | Date Considered 4/10/06 |
| *Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. | |
| Form PTO 1449 | Patent and Trademark Office - U.S. Department of Commerce |

* No MONTH cited in doc.

INFORMATION DISCLOSURE CITATION

| | | | |
|------------------|---------------|---------------|--------------|
| Atty. Docket No. | 4329.3299 | Appln. No. | 10/820,182 |
| Applicant | Sato et al. | Ex. A. Wilson | |
| Filing Date | April 8, 2004 | Group: | Unknown 2815 |



| U.S. PATENT DOCUMENTS | | | | | | | |
|-----------------------|-----------------|------------|------|-------|-----------|----------------------------|--|
| Examiner Initial* | Document Number | Issue Date | Name | Class | Sub Class | Filing Date If Appropriate | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

| FOREIGN PATENT DOCUMENTS | | | | | | | |
|--------------------------|-----------------|------------------|---------|-------|-----------|-----------------------|--|
| | Document Number | Publication Date | Country | Class | Sub Class | Translation Yes or No | |
| 0 No | 2003-31799 | 1/31/03 | Japan | | | No | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

| OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) | |
|--|--|
| 0 No | Monfray et al., "50nm - Gate All Around (GAA) - Silicon On Nothing (SON) - Devices: A Simple Way to Co-integration of GAA Transistors within bulk MOSFET process," Symposium on VLSI Technology Digest of Technical Papers (2002), pp. 108-109 No MONTH cited. |
| | |
| | |
| | |

| | | | |
|---|--------------------|---|---------|
| Examiner | <i>[Signature]</i> | Date Considered | 4/10/06 |
| *Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. | | | |
| Form PTO 1449 | | Patent and Trademark Office - U.S. Department of Commerce | |



OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

| | | | |
|------------------|--|-----------------|--------------------|
| Atty. Docket No. | 04329.3299 | Application No. | 10/820,182 |
| Applicants | Tsutomu SATO et al. <i>EX. A. Wilson</i> | | |
| Filing Date | April 8, 2004 | Group: | 281 1 5 |

U.S. PATENT DOCUMENTS

| Examiner Initial* | Document Number | Issue Date | Name | Class | Sub Class | Filing Date If Appropriate |
|-------------------|-----------------|------------|------|-------|-----------|----------------------------|
| <i>[initials]</i> | | | | | | |

FOREIGN PATENT DOCUMENTS

| Document Number | Publication Date | Country | Class | Sub Class | Translation Yes or No |
|-----------------|------------------|---------|-------|-----------|-----------------------|
| | | | | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

| | |
|-----------|---|
| <i>QW</i> | Sato et al., "A NEW SUBSTRATE ENGINEERING FOR THE FORMATION OF EMPTY SPACE IN SILICON (ESS) INDUCED BY SILICON SURFACE MIGRATION", International Electron Device Meeting, pps. 20.6.1-20.6.4, (1999). <i>Dec 1999</i> |
| <i>QW</i> | Sato et al., "FABRICATION OF SILICON-ON-NOTHING STRUCTURE BY SUBSTRATE ENGINEERING USING THE EMPTY-SPACE-IN-SILICON FORMATION TECHNIQUE", Japanese Journal of Applied Physics, Vol. 43, pps. 12-18, (2004). <i>JAN 2004</i> |
| | |
| | |

| | | | |
|---------------|--|---|----------------|
| Examiner | <i>[signature]</i> | Date Considered | <i>4/10/06</i> |
| *Examiner: | Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. | | |
| Form PTO 1449 | | Patent and Trademark Office - U.S. Department of Commerce | |